

REMARKS

Claims 1 and 2 are amended. New claims 3 – 18 are added. Support for the new and amended claims can be found, for example, at pages 6 – 7 and 14 – 15 of the specification as filed. No new matter is introduced.

The rejection of claims 1 and 2 under 35 USC 102(b) over Mori, US Patent 5,864,152 is respectfully traversed. Mori discloses a semiconductor memory device for storing data. As an initial matter, the memory devices in Mori appear to be based on double emitter transistors, rather than capacitors. (Col. 2, lines 44 – 56.) By contrast, the claimed invention provides a method and apparatus for storing data by accumulating charges in a capacitor.

The claimed invention also requires making a short circuit in a pair of bit lines in order to perform a precharge. Mori does not appear to describe or suggest this feature of the claimed invention. Applicants have reviewed Col 4, lines 56 – 67 as noted by the Examiner, but are uncertain how this section describes or suggests the creation of a short circuit between a pair of bit lines as required by the claimed invention. For at least these reasons, reconsideration and withdrawal of the rejection is respectfully requested.

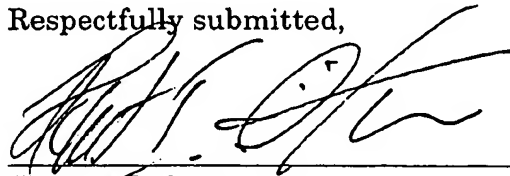
In view of the foregoing amendments and remarks, the application is respectfully submitted to be in condition for allowance, and prompt, favorable action thereon is earnestly solicited.

If there are any questions regarding this amendment or the application in general, a telephone call to the undersigned would be appreciated since this should expedite the prosecution of the application for all concerned.

If necessary to effect a timely response, this paper should be considered as a petition for an Extension of Time sufficient to effect a timely response, and please charge any deficiency in fees or credit any overpayments to Deposit Account No. 05-1323 (Docket #037133.52558US).

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Respectfully submitted,



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